CSCE 5615 Section 001 - Networks-on-Chip (Spring 2023 1)

CSCE 5615   Network-on-Chip

Spring 2023

Class Meetings: Tuesday 5:30-8:20 P.M. at Discovery Park B157

Instructor: Hui Zhao

Office Hours: By appointment

Email: Hui.Zhao@unt.edu

Office Hours: Tuesday 2-3 pm

Course Objectives

In this course, we will focus on the Network-on-Chip (NoC) design. The Network-on-Chip is a vital component in future many-core system-on-chips. To date, we are able to incorporate hundreds of cores into a single chip. However, we won't be able to benefit from such large amount of resources without providing efficient communication among them. Other than high speed communication, power and area overhead are also interconnection design bottlenecks. By taking this course, students will learn fundamental concepts in this area and be introduced to open questions that will not only help them improve their technical skills but also intrigue their interests in further research in computer system areas. Additionally, this course can also help students to develop topics of their Master's or Ph.D. thesis.

In this course, we will cover following topics of NoC design:

- Topology
- Router microarchitecture
- Flow control
- Routing algorithms
- Designing Power efficient NoC
- Emerging techniques in designing NoC

Text Book

There will be no required textbook.

Grading Policy (I reserve the rights to make changes to this policy)

- Homework/presentation: 30%
- Midterm: 35%
- Project: 30%
- Class participation: 5%

The exam will be held in class and will be closed book. The exam will test your understanding of the basic ideas and objectives of the class as covered in the course.

There are two options for the project: NoC simulation or paper survey. Students can choose to use NoC simulation tools developed in C/C++, or Verilog/VHDL to implement NoC design or perform a survey of NoC related topics.